IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Thomas, *et al.*	Docket No.:	INF 2003 P 54322 US
Serial No.:	10/790,907	Art Unit:	2822
Filed:	March 2, 2004	Examiner:	Bac H. Au
Title:	Integrated Circuit with Re-Route Layer and Stacked Die Assembly		

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

The Applicants wish to bring to the attention of the U.S. Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a, which may be considered material to the examination of the above-identified application. Copies of the U.S. Patents cited are not being submitted. However, the Applicants have included copies of the foreign patents.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(c)(1). Applicants hereby state that each item of information contained in this statement was first cited in a communication from a foreign patent office in a counterpart application not more than three months prior to the filing of this statement. As a result, no fee is due at this time.

Respectfully submitted,

27 Sept 2007
Date

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